ATTORNEY'S DOCKET NO: S1022.80363US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Geoff BARRETT
Serial No: 09/477,790   Patent No. 6,816,821 B1
Filed: December 31, 1999   Issued: November 9, 2004
For: POST IMAGE TECHNIQUES

Examiner: Herng Der Day
Art Unit: 2123   Confirmation No.   9742

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X]   Request for Certificate of Correction
[X]   Copies of: Pages 5 and 9 of Apl As Filed, Pages 3 and 8 from 12/08/03 Amend and Cols 4, 5 and 6 of U.S. 6,816,821.
[X]   PTO Form SB/44
[X]   Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 18 day of November, 2004.

Attorney Docket No.: S1022.80363US00
XNDD

Respectfully submitted,

Geoff Barrett, Patentee

By:
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DEC 0 3 2004

ATTORNEY'S DOCKET NO: S1022.80363US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Geoff BARRETT
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account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)   Respectfully submitted,

I hereby certify that this document is being placed in the
United States mail with first-class postage attached,   *Geoff Barrett, Patentee*
addressed to Certificate of Correction Branch, Commissioner
for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
the /8 day of November, 2004.

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ATTORNEY'S DOCKET NO: S1022.80363US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Geoff BARRETT
Serial No: 09/477,790   Patent No. 6,816,821 B1
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ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.322

Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, there is a typographical error and errors of omission in issued U.S. Patent No. 6,816,821.

In column 4, lines 7-10 currently read as shown below:

where I is an input and neither T0 nor T1 depend on 1, then I can be generated by parameterization of this equation to provide a new input J which satisfies the relation (Emphasis added)

However, on page 5 of the application as filed the same text reads:

where I is an input and neither T0 nor T1 depend on I, then I can be generated by parameterization of this equation to provide a new input J which satisfies the relation (Emphasis added)

The letter "1" identifying the input in issued U.S. Patent No. 6,816,821 is incorrect. As can be seen on page 5 of the application as filed, the letter "I" is used to identify the input. No amendment was made by either Patentee or the Examiner changing the "I" to "1".

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In column 6, lines 32-40 of issued U.S. Patent No. 6,816,821 currently read:

> A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the **second** system. This data is stored in fifth store 600. (Emphasis added)

However, in an amendment filed on December 8, 2003 the word "second" was replaced with the word "real." This paragraph found in column 5, lines 32-40, as amended should read as shown below.

> A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the **real** system. This data is stored in fifth store 600. (Emphasis added)

The final paragraph of the written description in column 6, lines 7-11, of U.S. Patent No. 6,816,821 reads:

> The above description is of preferred and exemplary embodiment(s) of the present invention only and is to enable a full understanding of the invention while not intending to limit the invention can be ascertained from the following claims.

At the time the application was filed, this paragraph found on page 9, lines 1-3, read as shown below:

> The above description is of preferred and exemplary embodiment(s) of the present invention only and is to enable a full understanding of the invention while not intending to limit the invention. **The scope of the invention** can be ascertained from the following claims:

No such amendment was made by either the Examiner or by Patentee deleting this text.

In support of this Request Patentee submits herewith a highlighted copy of pages 5 and 9 of the application as filed, pages 3 and 8 of the amendment filed on December 8, 2003 and columns 4, 5 and 6 of U.S. 6,816,821.

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Patentee requests that a Certificate of Correction be granted in U.S. Letters Patent No. 6,816,821 as specified herein and on the attached Certificate of Correction form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the corrections be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the ___ day of November, 2004.

Attorney Docket No.: S1022.80363US00US00
XNDD

Respectfully submitted,

Geoff Barrett, Patentee

By: _____

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FIG. 3 shows a conceptual flow diagram of a present technique.

In the figures, like reference numerals refer to like parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In this example, a two bit counter is used to demonstrate a technique for modeling a reverse machine. It will be clear to one skilled in the art that if the real machine is a conventional counter which counts up, then the reverse machine will be a machine which counts down.

It will also be clear to one skilled in the art that for the simplified examples selected here, properties would normally be proved by using only a pre-image calculation. Post-image calculation could be used for example to calculate the set of reachable states, namely all states which could be reached by a particular machine. In this situation, a typical method would be to start with a set of initial states, calculate the post-image and add the states resulting in the post-image to the original set. This would then be repeated until no new states were found and the resultant would be the set of reachable states.

Although it will be clear to one skilled in the art that for a two bit counter have states (0,0), (0,1), (1,0) and (1,1) the set of reachable states would comprise the set of all these states, the following description gives an example of the construction of a reverse machine which enables the use of pre-image calculation on that reverse machine to prove this.

Referring to FIG. 1, a two bit counter has four states S0, S1, S2 and S3. The transition from S0 to S1 is T01 the transition from state S1 to state S2 is T12, the transition from S2 to S3 is T23 and the transition from S3 to S0 is T30.

At state S0, the bits of the counter are both equal to zero (i.e. $b0=0$ and $b1=0$, where $b0$ is the least significant bit and $b1$ is the most significant bit). In state S1, the counter has $b0=1$ and $b1=0$, in state S2 $b0=0$ and $b1=1$, and in state S3 $b1=1$ and $b0=1$

The state transition functions are formed as follows:

1. For the least significant bit, a transition from one state to the next causes the least significant bit to be inverted, i.e. $b0=NOT\ b0$.

2. For the most significant bit, this has a value of logic 1, i.e. true where the previous state is S1 or S2. For S1, $b0$ is true and $b1$ is false and for S2 $b0$ is false and $b1$ is true. Thus,

$$b1=(NOT\ b0\ AND\ b1)\ OR\ (b0\ AND\ NOT\ b1).$$

As applied to this counter, an example of the use of the invention is to prove that only a transition from state S1 can directly result in state S2.

The invention accordingly provides a method and apparatus f or synthesizing a reverse model of a finite state machine. This will be demonstrated using the finite state machine shown in FIG. 1, i.e. synthesizing a reverse counter.

To do this, it is first necessary to note that for a reverse machine, transitions would take place in the reverse direction to those shown in FIG. 1. Thus, for the reverse machine, the next state of that reverse machine is in fact the previous state of the real machine. Thus, after a transition from $b0$ in the reverse machine, the result is a new value equal to $b0'$ and a transition in the reverse machine from $b1$ results in a new value of $b1'$ where the notation "'" indicates the previous state of the real machine.

Applying the transition functions of the real state machine to the transitions of the reverse machine to form constraints:

$$b0=NOT\ b0' \tag{1}$$

$$b1=(NOT\ b0'\ AND\ b1')\ OR\ (b0'\ AND\ NOT\ b1') \tag{2}$$

From our British Application No 9624935.4, which is incorporated by reference as if fully set forth herein, it was shown that if a constraint is given by

$$(NOT\ I\ AND\ T0)\ OR\ (I\ AND\ T1) \tag{3}$$

where I is an input and neither T0 nor T1 depend on 1, then I can be generated by parameterization of this equation to provide a new input J which satisfies the relation

$$I=(NOT\ J\ AND\ NOT\ T0)\ OR\ (J\ AND\ T1) \tag{4}$$

An equation for $b0'$ is now generated using the constraint (1) and the parameterization technique so that:

$$b0'=(NOT\ b0''\ AND\ NOT\ [b0=1])\ OR\ (b0''\ AND\ [b0=0])$$
$$=NOT\ b0$$

Substituting this equation in constraint (2) gives:

$$b1=(b0\ AND\ b1')\ OR\ (NOT\ b0\ AND\ NOT\ b1')\ or,$$
equivalently: [[-]]

$$(b1'[[)]]AND\ [b0=b1])\ OR\ (NOT\ b1'\ AND\ NOT\ [b0=b1])$$

By using this equation, an equation for $b1'$ can be generated by the parameterization technique, whereby:

$$b1'=(NOT\ b1''\ AND\ [b0=b1])\ OR\ (b1''\ AND\ [b0=b1])$$
thus $b1'=[b0=b1]$

The transitions of the reverse machine are now such that the value of $b0$ on the next cycle is calculated as NOT $b0$ and the value of $b1$ on the next cycle is calculated as $b0=b1$.

By substituting in the relationship (3) above:

$$b1'=(b0\ AND\ b1)\ or\ (NOT\ b0\ AND\ NOT\ b1).$$

Thus, the transition functions for the reverse machine give the following relationships: For bit 0: After a transition in the forward direction for the reverse machine, the new value of bit 0 will be true if the starting value of bit 0 were false.

In the context of the real machine, as has previously been explained, a forward transition of the reverse machine is identical to a reverse transition of the real machine. Thus, the above can be restated as:

The previous value of the bit 0 of the real machine is true if he·present value of bit 0 of the real machine is false.

For bit 1: Using the bit 0 relationship above: the previous value of bit 1 for the real machine is true if the present bit 0 and the present bit 1 are both true or if the present value of bit 0 and the 1present value of bit 1 are both false.

More generally, in a model checker based on the transition relation, the formula for the calculation of the post-image of a set of states is very similar to the formula for the calculation of the pre-image (pre(X)=∃S': X[S:=S'] & R and Post(X)=(∃S: X & R) [S':=S]), where the following notation applies:

X[V:=E] substitutes the expressions E for the variables V in the predicate (X)

∃V:X existential quantification of the variables V in the predicate X.

However, in a model checker based on transition functions, the post-image formula is complicated and difficult to implement efficiently. This section will show how to provide transition functions for the reverse machine (i.e. one in which transitions go from the current state to the previous state), and therefore the pre-image of the reverse system will be the post-image of the original system.

Let the state variables and transition functions of the machine be S and T (observation functions are not considered), then the reverse system is constructed as follows. First note that S' (the next-state variables of the reverse system) correspond to the previous states of the original

system. Beginning with the transitions of the reverse system being T', the transition functions of the original system are used to constrain them. Thus, for each state s and transition t, there is a constraint S=t[S:=S']. Call the set of constraints C. For each constraint, the parameterization E over the variables S', is calculated and this is substituted in the transition functions and the remaining constraints.

The parameterization is an idempotent parameterization i.e. a parameterization which after being affected, leaves the relationship entirely unaltered.

Referring to FIG. 2, a first store (memory) **100** stores bits representative of transition functions of a system. A second store **200** stores bits representative of estimated transition function of a reverse model of said system, the estimate being derived from knowledge of the next-state variables of the reverse system, which of course correspond to the previous state variables of the original system. A third store **300** stores bits representative of the set of state variables of the system, which necessarily is also the set of state variables of the reverse model.

A processor **400** has a logical transforming device **410** which receives the transition functions of the real machine from the first store **100** and transforms the transition functions into constraints on the reverse model. The processor further has a parameterization processing device **420** for calculating for each constraint the parameterization over the variables of the reverse machine which are then applied to the estimated transition functions of the reverse machine in applying means **430**. The applying means **430** provides an output to a fourth store **500** which stores the actual transition functions of the reverse model.

A processor **400** further includes a forming device **440** which receives the state variables of the real/reverse models from the third store **300** and also receives the transition functions of the reverse machine from the fourth store **500** and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the second system. This data is stored in fifth store **600**.

Referring to FIG. 3, the method of the invention, as described above, involves forming a model of the reverse machine and then applying as inputs to the model of the reverse machine, outputs of the real machine so as to determine what inputs in the real machine could give rise to those outputs. It is therefore necessary to provide an accurate model of the reverse machine and this part of the inventive method is shown in FIG. 3.

Referring to FIG. 3, a complete description of the real machine **1000** is accessed and processed to extract the state transitions **1002** using a processing engine **1001**. A second processing engine **1003** also accesses the description **1000** to provide the transition functions **1004** of the real machine. A further processing stage **1005** reverses the transitions of the real machine to provide an output **1006** of reverse transitions. The transition functions in box **1004** are processed **1007** to as to transform the transition functions of the real machine into constraints and a parameterization of the constraints is applied in stage **1008** to each and all of the reverse transitions to thereby form the model of the reverse machine **1010**. As reported above, by applying the outputs of the real machine as inputs to the model of the reverse machine, the inputs to the real machine can be discovered.

The described method and device has a large number of applications such as deriving properties of a control system using a model of the system or deriving properties of a hardware system using a model of the system. The described

novel technique may specifically be used for testing electronic circuits, testing logic circuits, including microprocessors. In general, the described method and device can be used for testing any mechanistic system in which states occur and transitions between the states occur on a clocked or a time-dependent basis.

The above description is of preferred and exemplary embodiment(s) of the present invention only and is to enable a full understanding of the invention while not intending to limit the invention can be ascertained from the following claims.

What is claimed is:

1. A method of synthesizing a reverse model of a finite state machine, the method comprising:

transforming a transition function of a state machine model of said finite state machine into a constraint on the reverse model, wherein the reverse model is a reverse model of the state machine model; and

applying a parameterization of said constraint to all transitions of the reverse model.

2. The method as claimed in claim 1 wherein said finite state machine includes a logic circuits.

3. The method as claimed in claim 1 wherein said finite state machine includes a microprocessor.

4. A method of calculating a post-image in a finite state machine, the method comprising:

forming a reverse model of said finite state machine, wherein the reverse model is a reverse model of a state machine model of the finite state machine; and

calculating a pre-image in said reverse model, wherein the pre-image in said reverse model is equivalent to the post-image in said finite state machine.

5. The method as claimed in claim 4 wherein said finite state machine includes a logic circuits.

6. The method as claimed in claim 4 wherein said finite state machine includes a microprocessor.

7. The method of claim 4 further comprising identifying from a characterization of a model of said finite state machine, transitions of said finite state machine and reversing said transitions to form potential transitions of a reverse model.

8. The method of claim 4 and further comprising extracting from a characterization of a model of said finite state machine, transition functions of said finite state machine.

9. A device for synthesizing a reverse model of a finite state machine, the device comprising:

a first store storing bits representative of transition functions of a state machine model of said finite state machine;

a second store storing bits representative of an estimate of transition functions of said reverse model; and

a processing system comprising

a logical device for transforming said transition functions of the state machine model of said finite state machine into constraints on said reverse model, wherein the reverse model is a reverse model of the state machine model; and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of said reverse model to form transition functions of said reverse model.

10. A device as claimed in claim 9 wherein said estimate of transition functions of said reverse model comprises previous state variables of said finite state machine.

11. The device as claimed in claim 9 wherein said finite state machine includes a logic circuits.

b1=(NOT b0 AND b1) OR (b0 AND NOT b1).

As applied to this counter, an example of the use of the invention is to prove that <u>only</u> a transition from state S1 can directly result in state S2.

The invention accordingly provides a method and apparatus f or synthesizing a reverse model of a finite state machine. This will be demonstrated using the finite state machine shown in Figure 1, i.e. synthesizing a reverse counter.

To do this, it is first necessary to note that for a reverse machine, transitions would take place in the reverse direction to those shown in Figure 1. Thus, for the reverse machine, the next state of that reverse machine is in fact the previous state of the real machine. Thus, after a transition from b0 in the reverse machine, the result is a new value equal to b0' and a transition in the reverse machine from b1 results in a new value of b1' where the notation " ' " indicates the previous state of the real machine.

Applying the transition functions of the real state machine to the transitions of the reverse machine to form constraints:

$$b0 = NOT\ b0' \tag{1}$$

$$b1 = (NOT\ b0'\ AND\ b1')\ OR\ (b0'\ AND\ NOT\ b1') \tag{2}$$

From our British Application No 9624935.4, which is incorporated by reference as if fully set forth herein, it was shown that if a constraint is given by
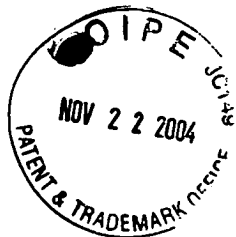
$$(NOT\ I\ AND\ T0)\ OR\ (I\ AND\ T1) \tag{3}$$

where I is an input and neither T0 nor T1 depend on I, then I can be generated by parameterization of this equation to provide a new input J which satisfies the relation

$$I = (NOT\ J\ AND\ NOT\ T0)\ OR\ (J\ AND\ T1) \tag{4}$$

An equation for b0' is now generated using the constraint (1) and the parameterization technique S0 that:

$$b0' = (NOT\ b0''\ AND\ NOT\ [b0=1])\ OR\ b0''\ AND\ [b0=0])$$

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The above description is of preferred and exemplary embodiment(s) of the present invention only and is to enable a full understanding of the invention while not intending to limit the invention. The scope of the invention can be ascertained from the following claims:

Serial No.: 09/477,790
Conf. No.: 9742

- 3 -

Art Unit: 2123

IN THE WRITTEN DESCRIPTION OF THE SPECIFICATION

Applicant presents a replacement paragraph below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. All references below to line numbers only include lines on which text is present.

Please rewrite the sentence beginning on page 8, line 4 to read as follows:

A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the ~~second~~ real system.

REMARKS

In response to the Office Action mailed July 8, 2003, Applicant respectfully requests reconsideration. To further the prosecution of the application, amendments have been made in the claims, the written description, and the drawings. The application as presented is believed to be in allowable condition.

IN THE DRAWINGS

In response to ¶ 3 of the Office Action, Applicant has modified Figure 3 to address the Draftsperson's objection that the lines, numbers and letters were not uniformly thick nor well defined. The line quality of Figure 3 has been improved to overcome the Draftsperson's rejection. No new matter has been added by this change. Applicant encloses a "Request for Corrections, Approval and Entry of Drawings" letter requesting the replacement of Figure 3 with the drawing in the Appendix of this response.

IN THE WRITTEN DESCRIPTION OF THE SPECIFICATION

In ¶ 4-1, the Office Action objects to the description at lines 7-9 of page 8. The specification has been amended at lines 7-9 of page 8 to remove the reference to a "second system" and to clarify that the sentence refers to a relationship between a reverse system and a real system. No new matter has been added by this amendment because the specification on page 7, lines 8-9 discloses that the pre-image of the reverse system will be the post-image of the original system and it is clear from Figure 3 that the original system refers to the real machine (i.e., the real system).

In ¶ 5, the Office Action objects to the incorporation by reference of Applicant's British application on page 5, stating that such incorporation is improper because it incorporates essential material. Applicant respectfully disagrees that any of the incorporated material is "essential," as none is necessary to describe or enable the claimed invention, nor to describe the best mode. MPEP § 608.01(p)(I)(A). Thus, Applicant's published British Application (No 9624935.4) is nonessential material and appropriate for incorporation by reference pursuant to MPEP § 608.01(p)(I)(A).

749569.3

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.   :   6,816,821 *B1*
DATED   :   November 9, 2004
INVENTOR(S)   :   Geoff Barret

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In col. 4, line 7 should read:

-- where I is an input and neither T0 nor T1 depend on I,--

In col. 5, line 7 should read:

-- of the reverse system thus the post-image of the real --

In col. 6, line 7 should read:

--limit the invention. The scope of the invention can be ascertained from the following--

MAILING ADDRESS OF SENDER   PATENT NO. 6,816,821 *B1*

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